CHAPTER 1

3D Integration for Semiconductor IC Packaging

1.1 Introduction

The electronics industry has been the largest industry since 1996 and may well reach 1.6 trillion dollars (i.e., $\$1.6 \times 10^{12}$) by the end of 2015. The most important invention of the electronics industry is, arguably, the transistor (1947), which earned John Bardeen, Walter Brattain, and William Shockley the Nobel Prize in 1956 for Physics. The invention of the IC (integrated circuit) by Jack Kilby in 1958 (which earned him the Nobel Prize in 2000 for Physics) and six months later by Robert Noyce (who did not share the Nobel Prize with Jack Kilby because he passed away in 1990) excited the generations of IC integrations.

The proposal of doubling the number of transistors on an IC chip (for minimum costs and innovations) every 24 months by Gordon Moore in 1965 (also called Moore's law) has been the most powerful driver for the development of the microelectronics industry in the past 50 years. This law emphasizes lithography scaling and integration (in 2D) of all functions on a single chip, perhaps through SoC (system-on-chip). On the other hand, the integration of all these functions can be achieved through 3D integration, which is the focus of this book.

1.2 3D Integration

3D integration consists of 3D IC packaging, 3D IC integration, and 3D Si integration, as shown in Fig. 1.1. They are different and in general the TSV (through-silicon via) separates 3D IC packaging from 3D IC integration and 3D Si integration since the latter two use TSV but 3D IC packaging does not.

TSV is the heart of 3D IC/Si integration. Figure 1.2 shows the U.S. patent (No. 3 044 909) "Semiconductive Wafer and Method of Making the Same" filed on October 23, 1958 and granted on July 17, 1962 by William Shockley. Yes, the same William Shockley who coinvented the greatest invention of all time in the semiconductor industry—the transistor.

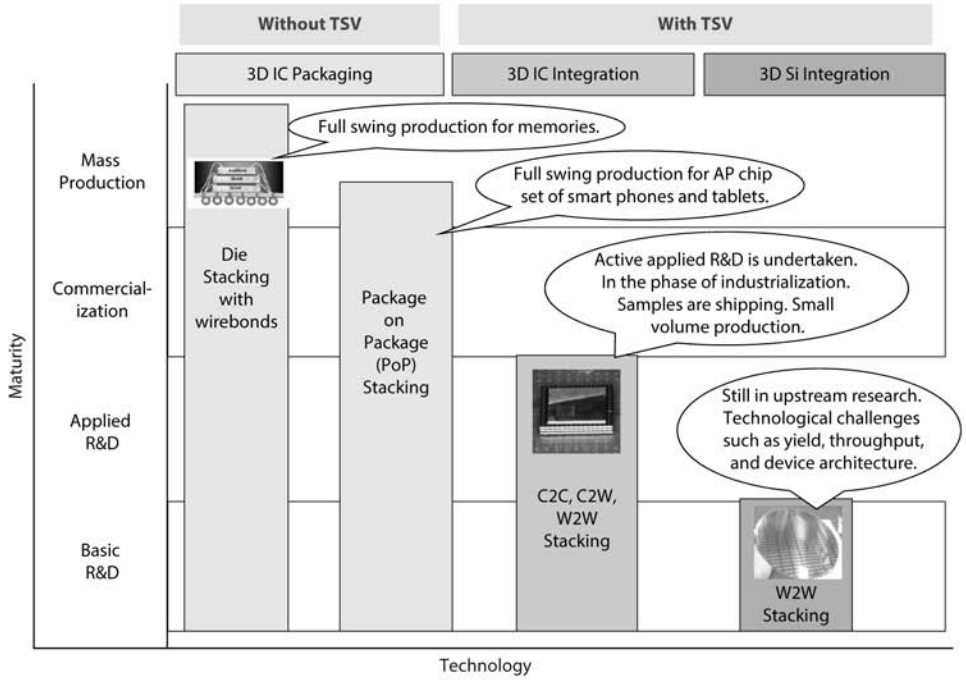


Figure 1.1 3D integration technology vs. maturity.

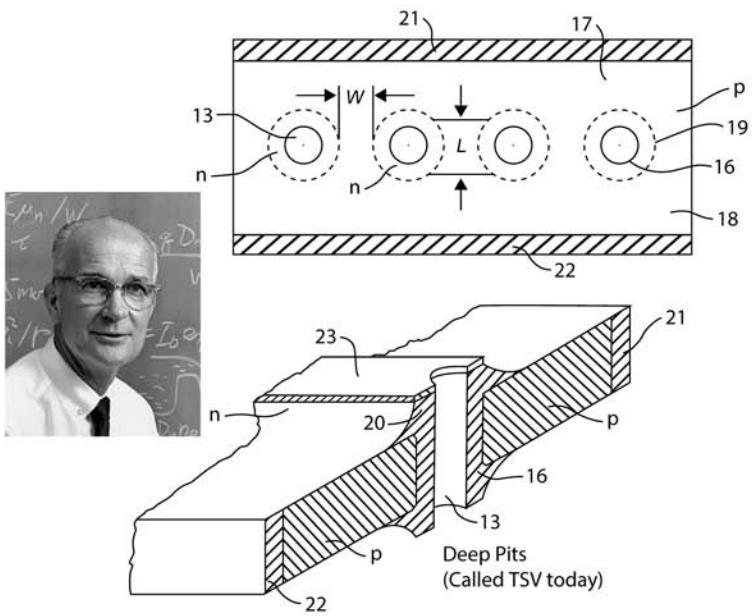


Figure 1.2 TSV invented by Shockley (U.S. patent #3 044 909).

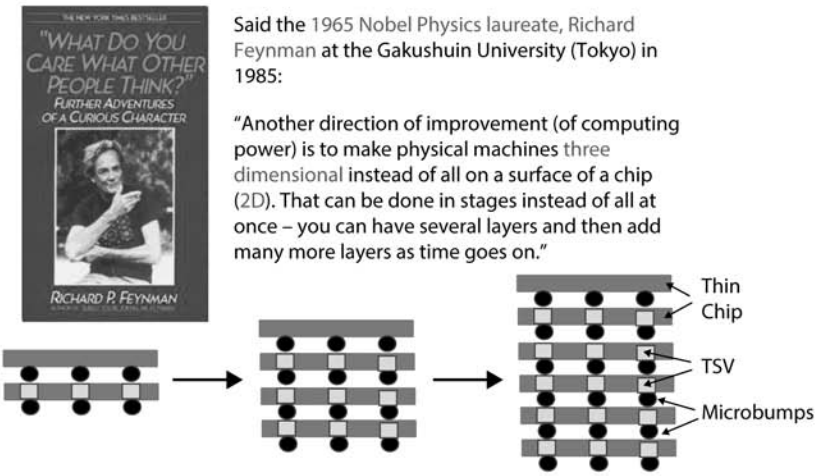


FIGURE 1.3 Richard Feynman, the most powerful promotor of 3D IC/Si integration.

Shockley invented TSV more than 50 years ago, but it was not meant for 3D IC/Si integration. 3D IC/Si integration [1–96] consists of two or more layers of active electronic components that are integrated vertically through TSVs into a single circuit. It was triggered by the advancement of the SOI (silicon-on-insulator) technology first reported by Gat and his colleagues [97], when people working in the field of semiconductors thought Moore's law would be hitting the wall by the 1990s. Of course, the facts showed otherwise.

The most powerful promotor of 3D IC/Si integration is the 1965 Nobel Physics laureate, Richard Feynman (Fig. 1.3). At the Nishina Memorial Lecture, *Computing Machines in the Future*, at Gakushuin University in Tokyo in 1985, he said, "Another direction of improvement (of computing power) is to make physical machines three dimensional instead of all on a surface of a chip. That can be done in stages instead of all at once—you can have several layers and then add many more layers as time goes on." Even today, many people who are searching for 3D IC/Si integration research funding like to cite his 1985 statement.

In the mid-1980s, the Japan MITI (Ministry of International Trade and Industry) funded and directed the 3D Research Committee of the 3D IC/Si integration project. Their road map is shown in Fig. 1.4 [78]. It was announced then that (1) functional models have been fabricated in stacked double or triple active layers demonstrating the concept of a future 3D structure, (2) the basic technology for stacking active layers will be developed before 1990, and (3) with this technology, various kinds of circuits such as high-packing density memory, high-speed logic, or image processors are expected to be designed and realized in a 3D single chip between 1990 and 2000. History showed that the technology did not materialize within the timeframe stated by the project.

In this chapter, 3D IC packaging, 3D IC integration, and 3D Si integration will be briefly mentioned. The supply chains for manufacturing the 3D IC integration will also be presented. Finally, the TSV manufacturing for CMOS image sensor and MEMS (microelectromechanical systems) will be briefly discussed.

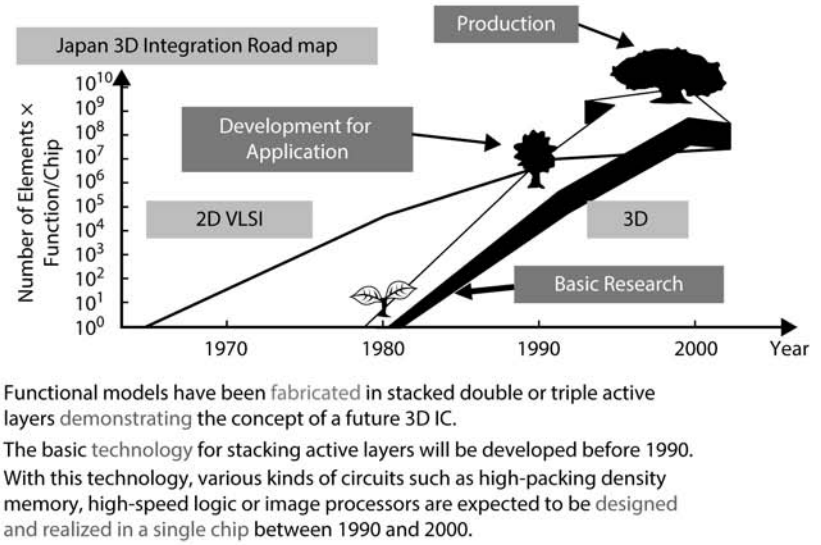


Figure 1.4 Japan 3D integration road map in the mid-1980s.

1.3 3D IC Packaging

3D IC packaging consists of two or more conventional components (packages) stacked in the vertical direction, as shown in Fig. 1.1. The most commons are chip stacking by wirebonding and PoP (package-on-package). One of the examples of chip stacking is stacking up memory chips with wirebonds and die attachments, as shown in Fig. 1.5. Today, 28 memory chips stacking are not uncommon. One of the examples of PoP is shown in Fig. 1.6, where a flip chip with solder bumps attached to a package substrate is supporting another package with cross-die wirebonding in the vertical direction.

3D memory chip stacking and PoP are mature technologies and in high-volume production as shown in the maturity status of 3D integration technology (Fig. 1.1), and thus

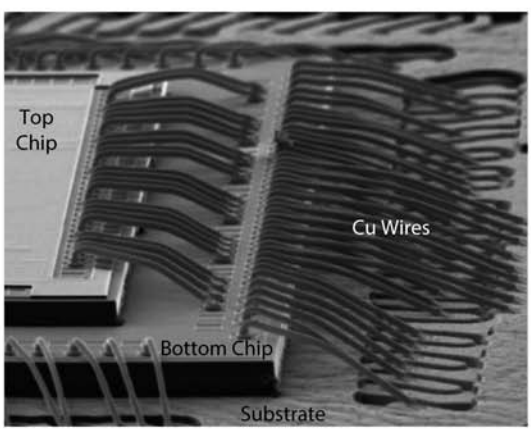


Figure 1.5 Amkor's chip stacking with Cu wirebonding.

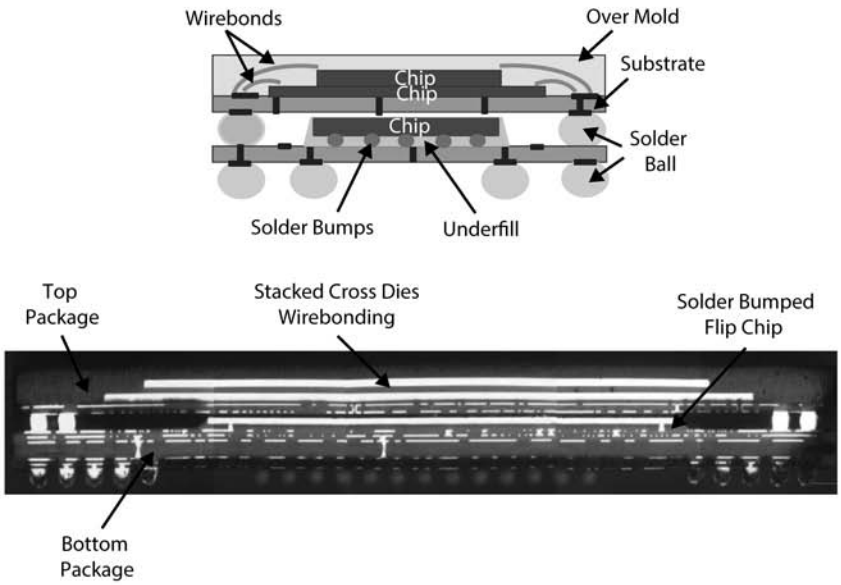


Figure 1.6 Package-on-package (PoP) for application processor chip set.

will not be discussed herein. However, 3D IC packaging technologies have been supporting mobile products such as smartphones and tablets and could be the main driver for materials consumption and new materials development for wearable products such as the smartwatch; they will be discussed in the last chapter of this book.

1.4 3D Si Integration

3D Si integration stacking up the wafers/chips in the vertical direction with TSVs but without any bumps (bumpless). Basically, W2W (wafer-to-wafer) is the only way to perform the bonding operation for 3D Si integration and yield is a big issue (e.g., some bad chips are forced to bond on the good chips). In addition, the absence of a gap (or an infinitesimal gap) between wafers and thermal management is a huge problem. Furthermore, the requirements of the bonding conditions, such as the surface cleanness, surface flatness, and class of clean room for 3D Si integration, are very high.

There are at least two different W2W bonding methods for 3D Si integration, namely, Cu-to-Cu bonding and oxide-to-oxide bonding, as shown in Figs. 1.7 and 1.8, respectively. Figure 1.7 shows a cross-section of the interface between the bumpless Cu-to-Cu electrodes (pads) given by the NIMS/AIST/Toshiba/University of Tokyo [79–85]. Figure 1.8 shows a cross-section of MIT's oxide-to-oxide bonding structure of three-layer 3D (ring oscillator) bonded at 275°C [86–92]. It can be seen that (1) the layers are bonded and interconnected with W-plugs, (2) the conventional inter-level connections are in the bottom two layers, and (3) the 3D vias are located in the isolation (field) region between transistors.

Tremendous amount of work still needs to be done before the products can be manufactured using the 3D Si integration technology. Besides thermal management, vias formation, thin-wafer handling, more research and development efforts should also be placed on areas

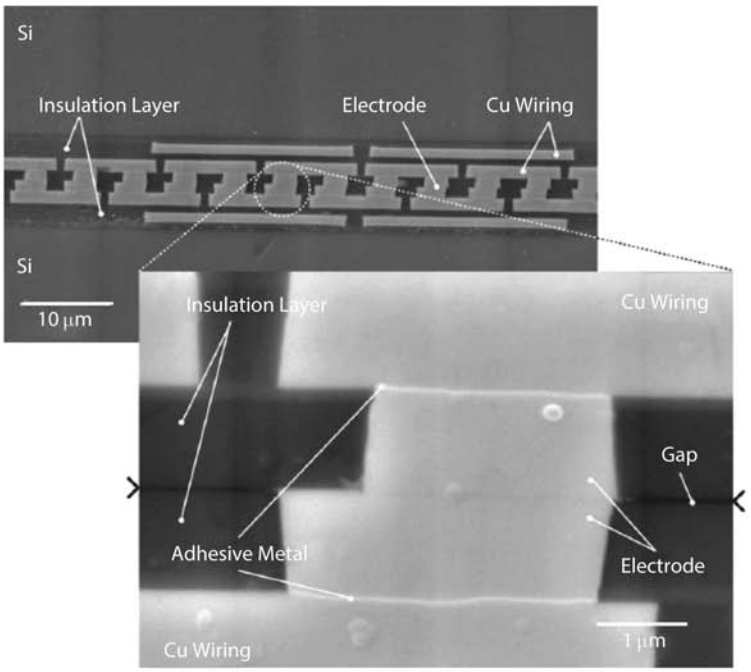


Figure 1.7 3D Si integration. NIMS/AIST/Toshiba/University of Tokyo's Cu-to-Cu bonding.

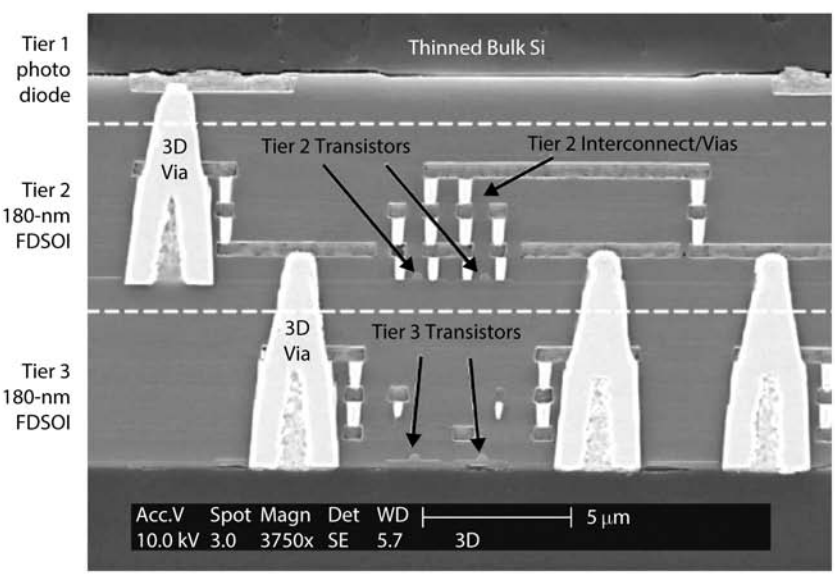


Figure 1.8 3D Si integration. MIT's oxide-to-oxide bonding.

such as cost reduction, design and process parameter optimization, bonding environment, W2W bonding alignment, wafer distortion, wafer bow (warpage), inspection and testing, contact performance, contact integrality, contact reliability, and manufacturing yield issues. In addition, packaging the 3D Si integration module systematically and reliably to the next level of interconnect poses another great challenge. Chapter 6 will present more information of 3D Si integration.

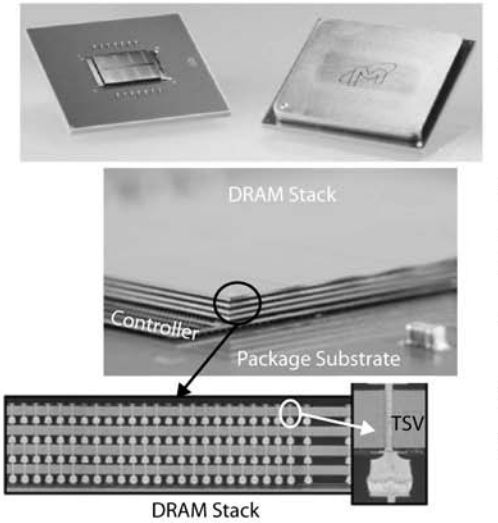
1.5 3D IC Integration

3D IC integration stacks up the thin chips in the vertical direction with TSVs and bumps. Unlike the conventional flip chip bumps (~100 μm), usually the 3D IC integration bumps are very small (<25 μm) and are called microbumps. The ones that are in and going into low-volume production are memory stacking with TSVs, HMC (hybrid memory cube) or wide I/O DRAM (dynamic random access memory), wide I/O DRAM 2, HBM (high bandwidth memory), and 2.5D IC integration (passive interposer).

Samsung mass-produced (August 2014) the industry's first TSV-based 64-GB DDR4 (double data rate type 4) DRAM module (memory stacking with TSVs), which consists of 36 DDR4 DRAM chips, each of which consists of four 4-GB DDR4 DRAM dies. The module performs twice as fast as a module that uses wirebonding packaging, while consuming approximately half the power. The module is for server application.

1.5.1 Hybrid Memory Cube

Figure 1.9 shows the very first sample shipped by Micron/IBM at the end of September 2013. It is an HMC that consists of 4 DRAMs each with 2000+ TSVs sacking on top of a logic controller with TSVs. The TSV DRAM cube is fabricated by Micron and the TSV controller is fabricated by IBM. The microbumps are Cu pillars (20 μm tall) with solder caps. Altera has designed a demonstration board for the HMC and Altera FPGAs.



- The hybrid memory cube is a 4-DRAM (each one with 2000+ TSVs) on a logic controller (which size is slightly larger than the DRAMs) with TSVs.
- The hybrid memory cube is on an organic package substrate.
- The TSV-DRAM is ~50 μm thick.
- The TSV-DRAM is with 20-μm (tall) Cu pillar + solder cap.
- The memory cube is assembled one DRAM at a time with thermal compression bonding.
- The heat dissipation is from 10 to 20 W.
- TSV diameter ~5 to 6 μm.

Figure 1.9 Micron's sample on hybrid memory cube (HMC).

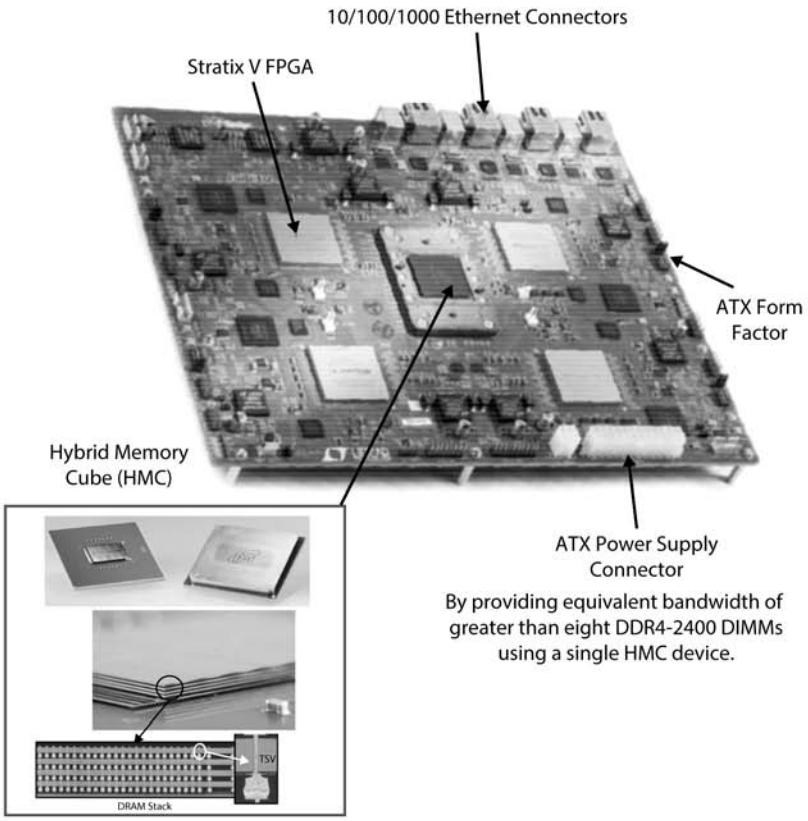


Figure 1.10 Altera FPGAs and HMC.

Figure 1.10 shows the platform using Altera's flagship 28-nm Stratix V FPGA (field programmable gate array) to interoperate with an HMC device [93]. It proves the technology leadership in the memory domain by providing equivalent bandwidth of greater than eight DDR4-2400 DIMMs (dual in-line memory modules) using a single HMC device. Figure 1.11 schematically shows Intel's 72-core "Knights Landing" Xeon Phi coprocessor with the HMCs [94]. Micron reports that having such memory in the CPU package is expected to deliver five times the sustained memory bandwidth versus GDDR5 (graphic double data rate type 5) with one-third the energy per bit in half the footprint. Figure 1.12 shows Fujitsu's microprocessors with HMCs for their supercomputer [95]. The HMCs deliver faster throughout and much better power utilization.

1.5.2 Wide I/O DRAM and Wide I/O 2

JEDEC standard JESD229, *Wide I/O SDR (Wide I/O Single Data Rate)*, was published in December 2011 and JEDEC standard JESD229-2, *Wide I/O 2 (WideI/O2)*, was published in August 2014.

They are meant for a stack of DRAMs with TSVs on a logic controller with TSVs; very similar to the HMC. The microbumps are divided into four quadrants with signal

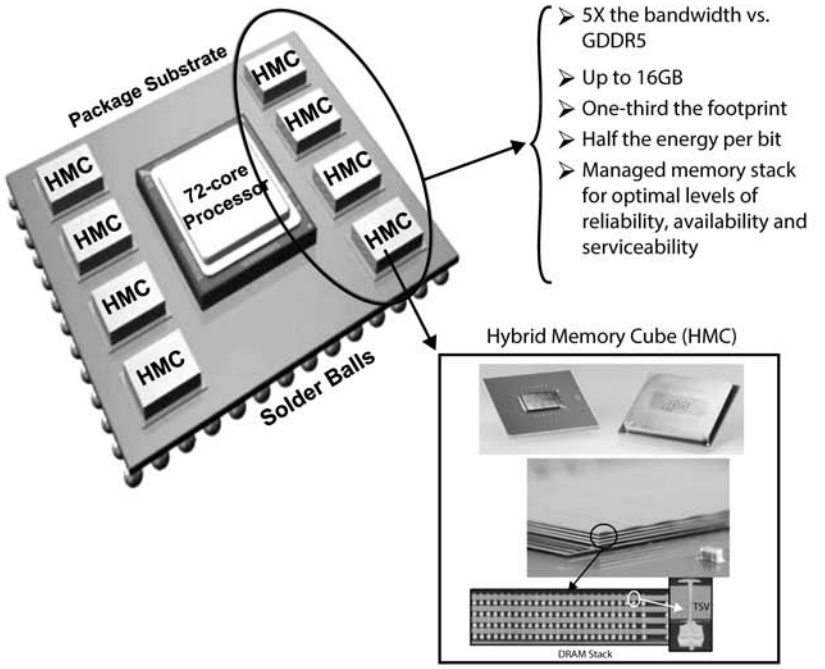


Figure 1.11 Intel's "Knight's Landing" with eight HMCs.

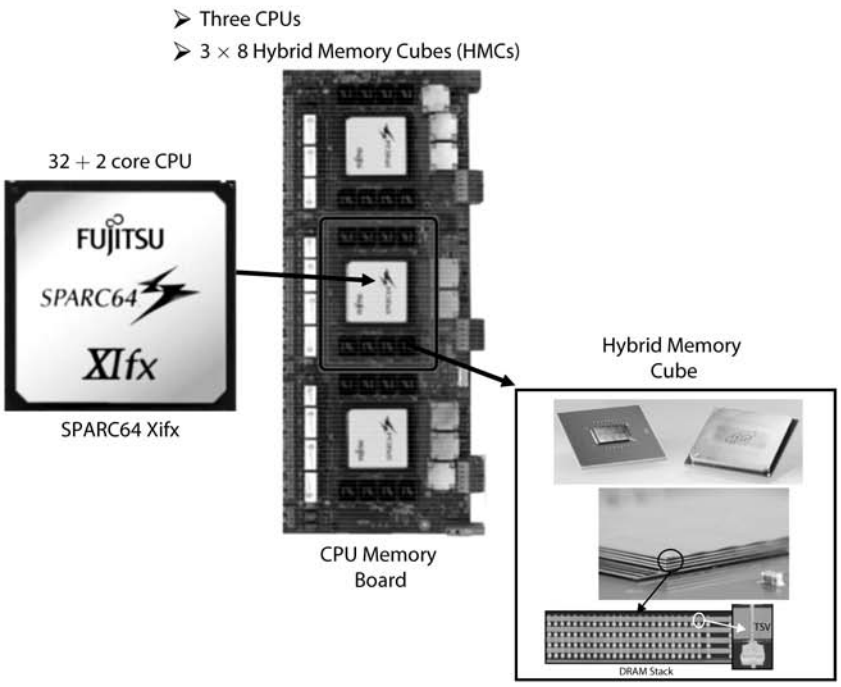


Figure 1.12 Fujitsu's CPU with HMCs.

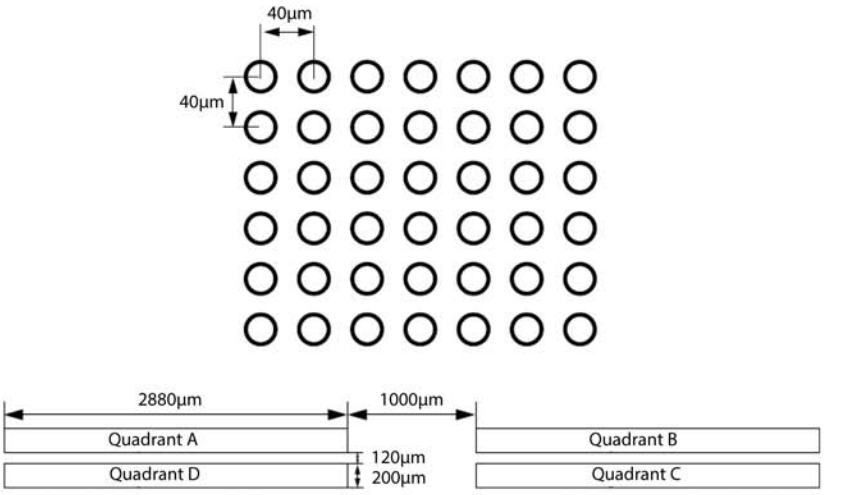


Figure 1.13 Wide I/O 2.

assignments mirrored both horizontally and vertically, as shown in Fig. 1.13, where the bump pitch (40 µm) of the area array is also shown. The dimensions of each quadrant are 2880 µm × 200 µm. There will be a space between quadrants in the x-direction (1000 µm) and in the y-direction (120 µm).

1.5.3 High Bandwidth Memory

Figure 1.14 shows schematically a HBM system by Hynix/AMD, which is based on JEDEC standard JESD235, *HBM DRAM*, published in December 2013. It is meant for graphics applications supporting bandwidth from 128 to 256 GB/s. A TSV/RDL interposer is used to support/connect mainly the lateral communication (HBM interface) between the HBM DRAM memory cube with TSVs and the GPU (graphic processor unit) or CPU (central processor unit) without TSVs. The optional base chip is used for buffering and signal rerouting of the HBM DRAM cube.

1.5.4 Wide I/O Memory (or Logic-on-Logic)

Figure 1.15 shows a wide I/O memory sample made by Samsung. It consists of a wide bandwidth low-power consumption memory chip with 1000+ of I/Os and is right on top of a logic chip with TSVs. The memory chip can also be a logic chip, then it will become a logic-on-logic. The wide I/O memory or logic-on-logic is supporting by an organic package substrate.

1.5.5 Passive Interposer (2.5D IC Integration)

A 2.5D integration is a TSV interposer system that consists of a piece of device-less silicon with TSVs and high-performance, high-density, fine-pitch IC chips without TSV. This piece of device-less silicon (also called a passive interposer) is used to support the chips and has RDLs (mainly) for lateral communication between the chips, as shown schematically in

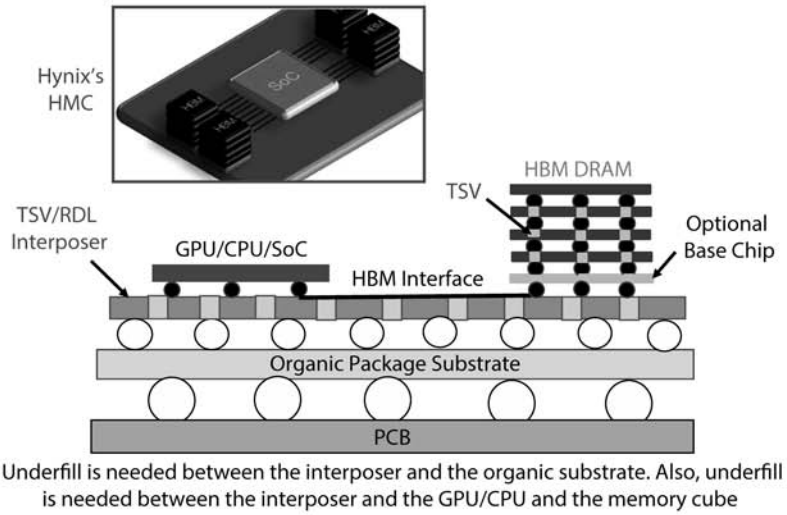


Figure 1.14 High Bandwidth Memory (HBM).

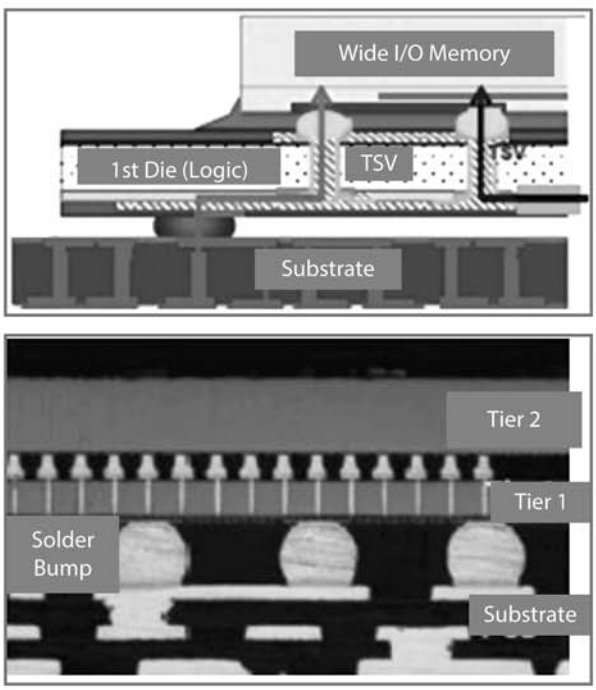


Figure 1.15 Wide I/O memory (or logic-on-logic).

Fig. 1.16. Figure 1.17 shows a sample designed by Xilinx and fabricated by TSMC. It can be seen that even with more than 10 Build-up layers on the package substrate, it is still not enough to support the four 28 nm FPGA chips. In addition, a passive TSV interposer with 200,000+ microbumps on 45 μm pitch and four RDLs (three Cu damascene layers and one aluminum layer) at a minimum of 0.4 μm pitch is needed. This type of structure (Figs. 1.16 and 1.17) is called by TSMC as chip on (interposer) wafer on (package) substrate (CoWoS) and has been in small-volume production since early 2013.

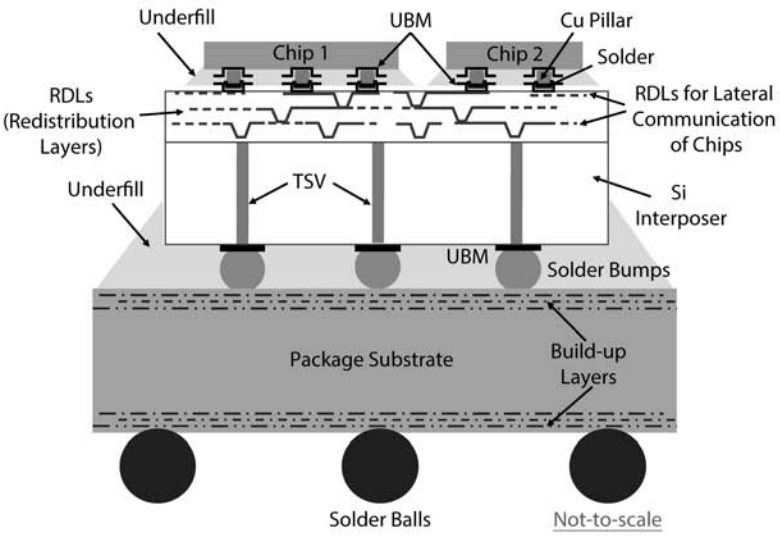


Figure 1.16 TSV/RDL passive interposer supporting chips on package substrate.

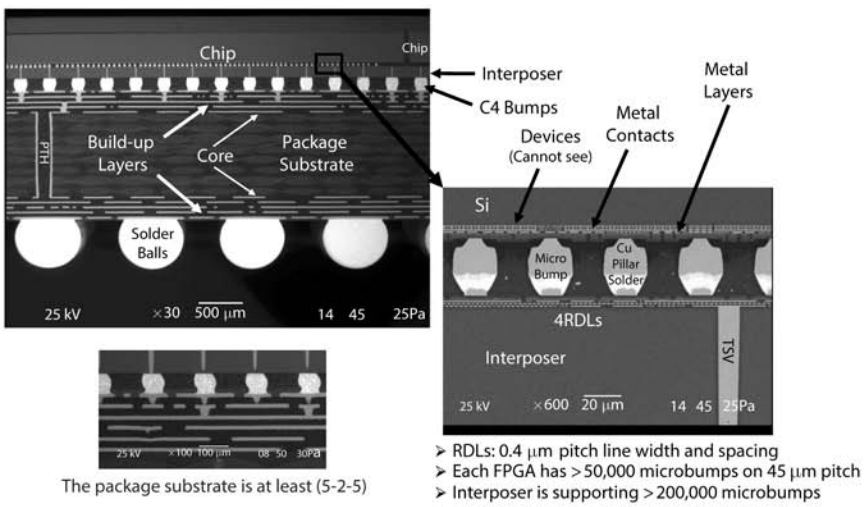


Figure 1.17 Xilinx/TSMC chip on wafer on substrate.

1.6 Supply Chains before the TSV Era

Before the TSV era, the technology supply chains are very well defined and understood. Descriptions of the various entities comprising the supply chain before the TSV era are presented below.

1.6.1 FEOL (Front-End-of-Line)

This is the first portion of IC fabrication where the individual devices such as transistors or resistors are patterned. This process is from a bare wafer to (but not including) the deposition of metal layers. FEOL is usually performed in semiconductor fabrication plants (fabs).

1.6.2 BEOL (Back-End-of-Line)

This is the fabrication in which active devices are interconnected with wiring on the wafer. This process starts from the first layer of metal to bonding pads with passivation. It also includes insulators and metal contacts and is called MOL (middle-of-the-line). The term "MOL" is seldom used and embedded in the BEOL. Again, BEOL is usually performed in the fab.

1.6.3 OSAT (Outsourced Semiconductor Assembly and Test)

This term is also called packaging, assembly and test. The process starts when the passivated wafer is received from the fab and then goes through circuit probing, bumping, thinning, dicing, wiring bonding, flip chip, molding, ball mounting, final testing, and etc.

1.7 Supply Chains for the TSV Era—Who Makes the TSV?

The following steps in the TSV fabrication process impact the various considerations that must be addressed.

1.7.1 TSVs Fabricated by the Via-First Process

The TSVs are fabricated before the FEOL. This can only be done by the fab. However, even in the fab, this seldom happens because the devices (e.g., transistors) are much more important than the TSVs.

1.7.2 TSVs Fabricated by the Via-Middle Process

The TSVs are fabricated right after the FEOL (e.g., transistors) and MOL (e.g., metal contacts), and before the BEOL (e.g., metal layers). In this case, the MOL is no longer embedded in the BEOL because the TSV fabrication process is between them. Owing to logistics and equipment compatibilities, usually the TSV by the via-middle process is done by the fab. For more information, please see Sec. 7.2.3.

1.7.3 TSVs Fabricated by the Via-Last (from the Front Side) Process

The TSVs are fabricated (from the front side of the wafer) after the FEOL, MOL, and BEOL. As of today, there is not a single creditable paper published with this process.

1.7.4 TSVs Fabricated by the Via-Last (from the Back Side) Process

The TSVs are fabricated (from the back side of the wafer) after the FEOL, MOL, and BEOL processes. The CMOS image sensor is an example. Strictly speaking, CMOS image sensors are not examples of 3D IC integration. For CMOS device sample wafers, the only creditable

publication is given by LETI et al. [96]. However, due to the technical issues, such as hitting the various embedded alignment targets in the x-, y- and z-directions (to enable the alignment between the metal layers on the top side of the wafer and the positioning of TSVs formed from the back side), TSVs fabricated by the via-last (from the back side) process should be avoided until these issues are resolved. For more information, please see Sec. 7.2.5.

Based on the above discussions, it seems that for active device wafers being used for 3D IC integration applications, TSVs are better fabricated using the via-middle process. Also, the TSVs should be fabricated by the fab, where all the equipment and expertise already exist and the cost to fabricate the TSVs is less than 5% of the cost in fabricating the ($\leqslant$32 nm) device wafers!

1.7.5 How About the Passive TSV Interposers?

When the industry defined the TSV processes for 3D IC integration, there were no passive interposers yet. Also, since there is no active device in the passive interposers, thus they do not fit into any of the preceding!

1.7.6 Who Wants to Fabricate the TSV for Passive Interposers?

Both the fab and OSAT want to do it! It depends on the layout, design, and fabrication capabilities, especially the line width and spacing of the RDLs. Usually, a few microns of line width and spacing can be done by the OSAT. Otherwise, it should be done by the fab.

1.7.7 Summary and Recommendations

The supply chains for making the TSV have been presented. Some important results and recommendations are summarized as follows:

For device wafers and high volume manufacturing, the TSVs should be fabricated by the foundries and with the via-middle process.

For dummy (deviceless) wafers, TSVs can be done by either the foundries or OSAT. For $\geqslant$3 μm line width and spacing RDLs and $\geqslant$5 μm-diameter vias, either the fab or the OSAT can do it. Otherwise, it should be done by the fab.

1.8 Supply Chains for the TSV Era—Who Does the MEOL, Assembly, and Test?

All the TSVs fabricated are blind vias. The blind TSV wafer is followed by solder bumping, temporary bonding, back grinding, TSV revealing, thin wafer handling, debonding, cleaning, etc. that, taken together, are called MEOL (middle-end-of-line). In this section, except for the vertically integrated companies (e.g., TSMC and Samsung), it is better for the MEOL process flow to be performed by the OSAT. The critical steps (including FEOL, MOL, BEOL, TSV, MEOL, assembly and test) and their ownership for making some of the 3D IC integrations are shown in the following sections.

1.8.1 Wide I/O Memory (Face-to-Back) by TSV Via-Middle Fabrication Process

Figure 1.18 shows the critical steps and ownerships for processing the logic wafer. After FEOL (to pattern the devices) and MOL (to make the metal contacts), the TSVs are fabricated by five key steps, namely via formation by deep reactive ion etch, dielectric deposition by plasma enhance chemical vapor deposition, barrier and seed layer by physical vapor deposition, Cu-filling by electroplating, Cu annealing, and CMP (chemical mechanical polishing) to

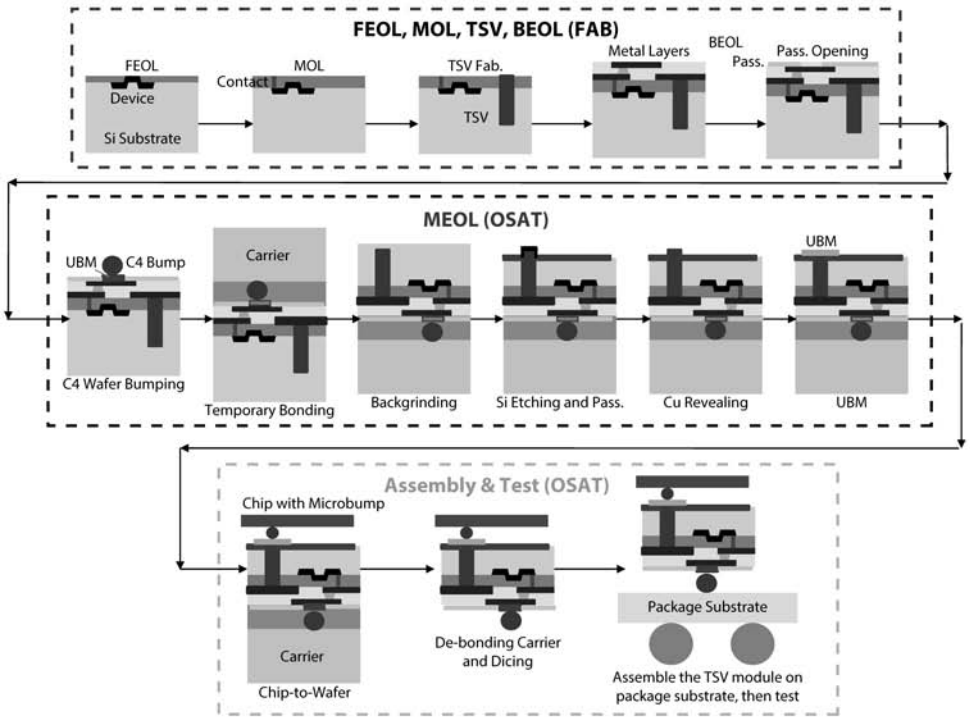


Figure 1.18 Critical steps and ownerships for (face-to-back) wide I/O memory using the TSV via-middle fabrication process.

remove the overburden Cu. These steps are then followed by the buildup of the metal layers, and finally, the passivation/openings (BEOL). All these steps should be done in the fab.

The MEOL starts off by UBM (under bump metallization) and C4 (controlled-collapse chip connection) ordinary wafer bumping with solder to the whole logic wafer. It is followed by temporary bonding of the TSV wafer to a supporting (carrier) wafer with adhesive. Then back grind the TSV wafer to a few microns from the tip of the Cu-filled TSV. It is followed by silicon dry etching to a few microns below the tip of the Cu-filled TSV. After that, a low temperature isolation SiN/SiO_2 deposition is applied to the whole wafer. Then CMP is used to remove the SiN/SiO_2 and the Cu and seed layers of the Cu-filled TSV (Cu revealing). Finally, an UBM is built on the tip of the Cu-filled TSV. All these steps should be done by the OSAT (except for vertical integrated foundries).

Separately, the memory wafer is microbumped with tiny solder bumps or Cu-pillars with solder caps. Then the wafer is diced into individual chips with microbumps/Cu-pillars. These steps also should be done by the OSAT.

Next is C2W (chip-to-wafer) bonding, i.e., the microbumped memory chip is bonded (either by natural reflow or thermal compression) to the TSV wafer with the carrier. After face-to-back C2W bonding, the carrier wafer is debonded from the TSV wafer. It is followed by dicing the TSV wafer into individual TSV modules. This TSV module is solder (natural) reflowed on a package substrate, and then tested. All these C2W bonding, dicing, assembly, and testing steps should be done by the OSAT.

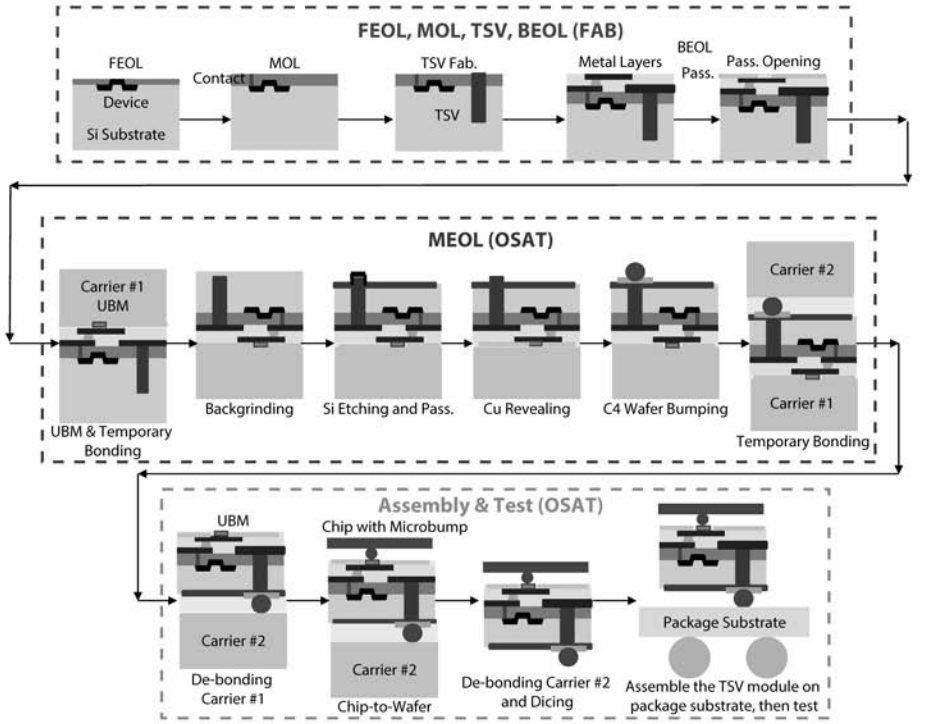


Figure 1.19 Critical steps and ownerships for (face-to-face) wide I/O memory using the TSV via-middle fabrication process.

1.8.2 Wide I/O Memory (Face-to-Face) by TSV Via-Middle Fabrication Process

The FEOL, MOL, TSV, and BEOL processes are exactly the same as those done in the TSV via-middle (face-to-back) process. However, the processes that follow it are different. Instead of C4 ordinary wafer bumping with solder after the UBM, the TSV wafer is temporarily bonded to carrier #1. Then, back grind the TSV wafer, reveal the Cu TSV, and fabricate the UBM. Those steps are followed by C4 ordinary wafer bumping with solder and temporary bonding to carrier #2. Then carrier #1 is debonded from the TSV wafer and C2W (face-to-face) bonding is performed. After C2W bonding, the carrier #2 is debonded from the TSV wafer. It is followed by dicing the TSV wafer into individual TSV modules. This TSV module is solder reflowed on a package substrate, then tested. The critical steps and their ownerships are shown in Fig. 1.19.

1.8.3 Wide I/O DRAM by TSV Via-Middle Fabrication Process

After FEOL, MOL, TSV, and BEOL of the logic and DRAM wafers, the SoC/logic wafer will go through the same steps, as shown in Fig. 1.18 for face-to-back, or Fig. 1.19 for face-to-face. For the DRAMs, UBM is done first followed by microwafer bumping of the whole wafer. These processes are then followed by temporary bonding to a carrier wafer, back grinding, Cu revealing, and UBM. These in turn are followed by debonding of the carrier wafer and dicing of the TSV DRAM wafer into individual TSV DRAM chips, as shown in Fig. 1.20.

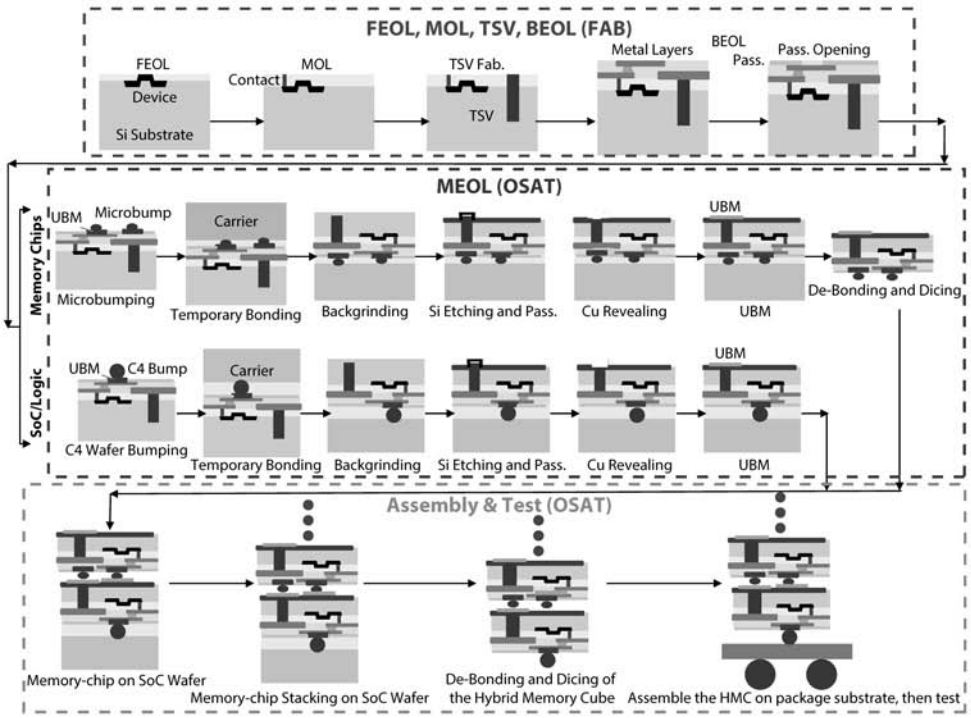


Figure 1.20 Critical steps and ownerships for wide I/O DRAM using the TSV via-middle fabrication process.

The next process is C2W (DRAM chip to logic wafer) bonding (e.g., 2-stacking, 4-stacking, 6-stacking or 8-stacking). After C2W bonding, the carrier wafer is debonded from the logic wafer and diced into individual HMCs (DRAM-stacking + logic). These steps are followed by assembly of the HMC with over-mold + underfill on a package substrate, and finally testing.

1.8.4 2.5D IC Integration with TSV/RDL Passive Interposers

Figure 1.21 shows the critical steps and their ownerships. After the deposition of a passivation layer on a piece of dummy silicon (no active devices), the TSV can be fabricated, RDL can be built, and passivation/openings can be made. After the UBM, the TSV wafer is temporarily bonded to carrier #1. It is followed by back grinding, silicon etching, low-temperature passivation, and Cu revealing. Then, UBM, C4 wafer bumping with solder, and temporary bonding to carrier #2 are accomplished.

Separately, the device wafer without TSVs is subjected to either microbumping with tiny solder bumps or Cu-pillars with solder caps. The device wafer is then diced into individual chips with microbumps/Cu-pillars.

The next processes to be accomplished are debonding of carrier #1, performing C2W bonding (the device chip to the TSV wafer). After C2W bonding, carrier #2 is debonded and the TSV wafer is diced into individual TSV modules. Finally, the TSV module can be assembled on a package substrate, and then tested.

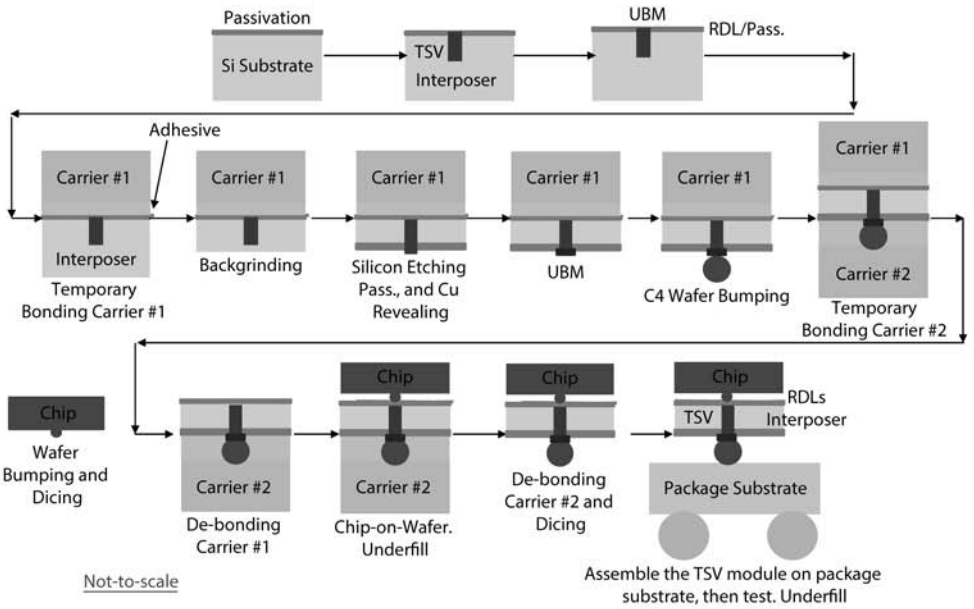


Figure 1.21 Critical steps and ownerships for 2.5D IC integration with a TSV/RDL passive interposer.

It can be seen from Fig. 1.21 that the TSV and RDL can be made by either the fab or the OSAT. It depends on the layout, design, and fabrication capabilities, especially the line width and spacing of the RDLs. Usually, a few microns of line width and spacing can be done by the OSAT. Otherwise, it should be done by the fab.

Except vertically integrated companies, such as TSMC, who want to do the CoWoS process completely in house, most fabless design houses prefer the fab (e.g., UMC and GlobalFoundries) to make the blind TSVs and the RDLs of the passive interposer. Then, the fabs hand the unfinished "TSV interposer" off to an OSAT for MEOL (solder bumping/temporary bonding/thin wafer handling/back grinding/TSV revealing/debonding/cleaning), assembly and test. This is also true for the unfinished TSV device wafers.

1.8.5 Summary and Recommendations

The technology supply chains for 2.5D/3D IC integration manufacturing have been presented. Critical steps such as FEOL, MOL, BEOL, TSV, MEOL, assembly and test, and their ownerships for potential applications and HVM of 2.5D/3D IC integrations such as wide I/O memory (or logic-on-logic), wide I/O DRAM (or HMC), and passive interposer (or 2.5D IC integration) have also been provided and discussed. Some important results and recommendations are summarized as follows:

For both device wafers and passive interposer wafers and high volume manufacturing, the MEOL, assembly and test processes should be done by the OSAT (except vertically integrated companies).

It can be seen from Fig. 1.18 through Fig. 1.21 that there are many important steps in the MEOL (solder bumping/temporary bonding/back grinding/TSV Cu revealing/thin

wafer handling/debonding/cleaning), assembly and test; therefore, the OSATs should strive to make themselves ready for a robust and high-yielding manufacturing process.

In order to have a smooth hand-off from the fab to the OSAT of the unfinished TSV wafer, more research and development work should be performed on the testing methods for blind TSV wafers for electrical [27, 51], thermal [61], and mechanical performance.

1.9 CMOS Images Sensors with TSVs

1.9.1 Toshiba's Dynastron™

In 2008, Toshiba produced their CMOS image sensor (CIS) with TSVs. Actually, Toshiba did not call it TSV but TCV (through chip via). In order to reduce the size of the product, they replaced the wirebonding COB (chip on board) technology of their CMOS image sensor into solder bumped flip chip technology. In order for the signals from the board to reach the pads of the sensor, they made the TCV, as shown in Fig. 1.22.

1.9.2 STMicroelectronics' VGA CIS Camera Module

In 2009, STMicroelectronics produced their VGA (video graphics array) CIS. They integrated the 2.2-μm pixel CIS into Nokia 2330 camera module, as shown in Fig. 1.23. The CIS chip is manufactured by a CMOS technology with a 0.18 μm process technology. The CIS module is wafer-level packaged using a via-last TSV process.

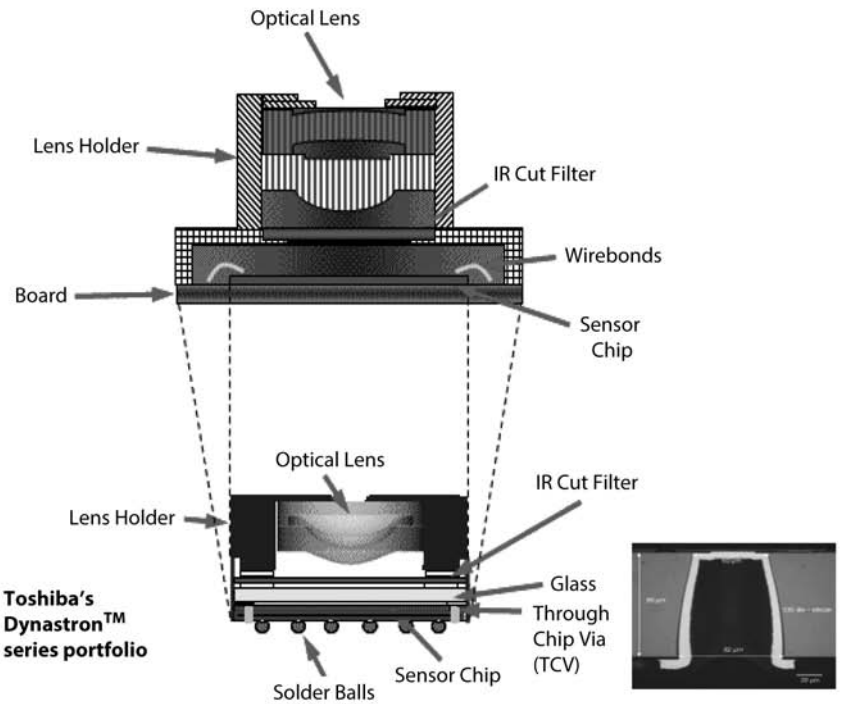


Figure 1.22 Toshiba's Dynastron™ with TSV (2008).

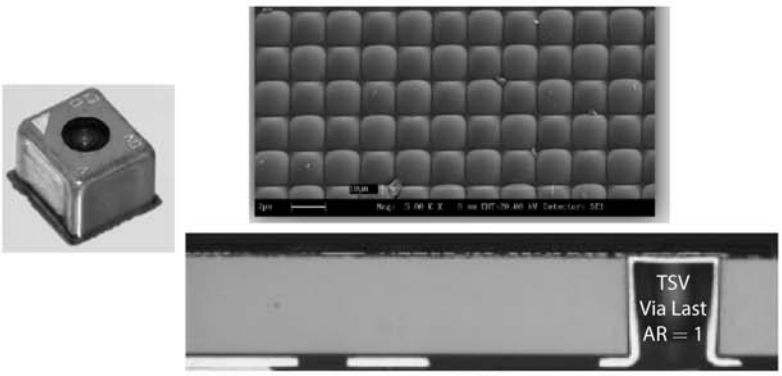


Figure 1.23 STMicroelectronics's VGA CIS Camera Module with TSV (2009).

1.9.3 Samsung's S5K4E5YX BSI CIS

In 2010 Samsung produced their S5K4E5YX 5.1Mp, 1/4.1" optical format 1.4 μm pixel pitch BSI (back side illuminated) CIS. The TSV with a BSI substrate serves to redistribute a back bond pad metallization through the substrate to the front metallization, as shown in Fig. 1.24.

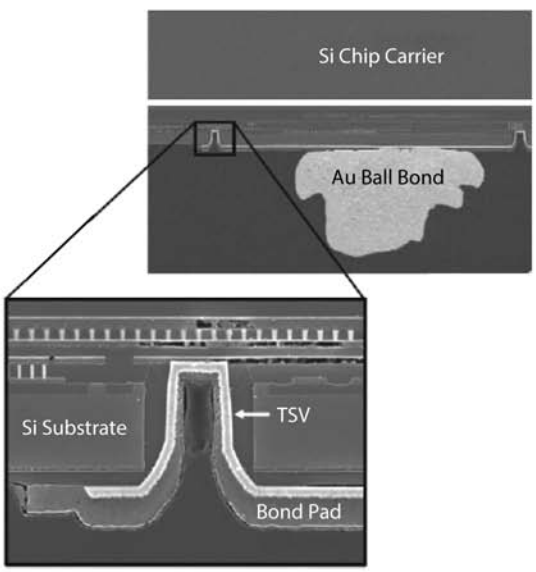


Figure 1.24 Samsung's S5K4E5YX BSI CIS with TSV (2010).

1.9.4 Toshiba's HEW4 BSI TCM5103PL

In 2011 Toshiba produced the HEW4 BSI TCM5103PL 16Mp, 1.4 μm pixel pitch CIS. Its cross-section is shown in Fig. 1.25. It can be seen that (a) the TSV diameter is ~0.5 μm and